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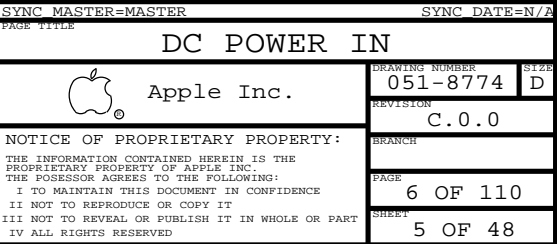
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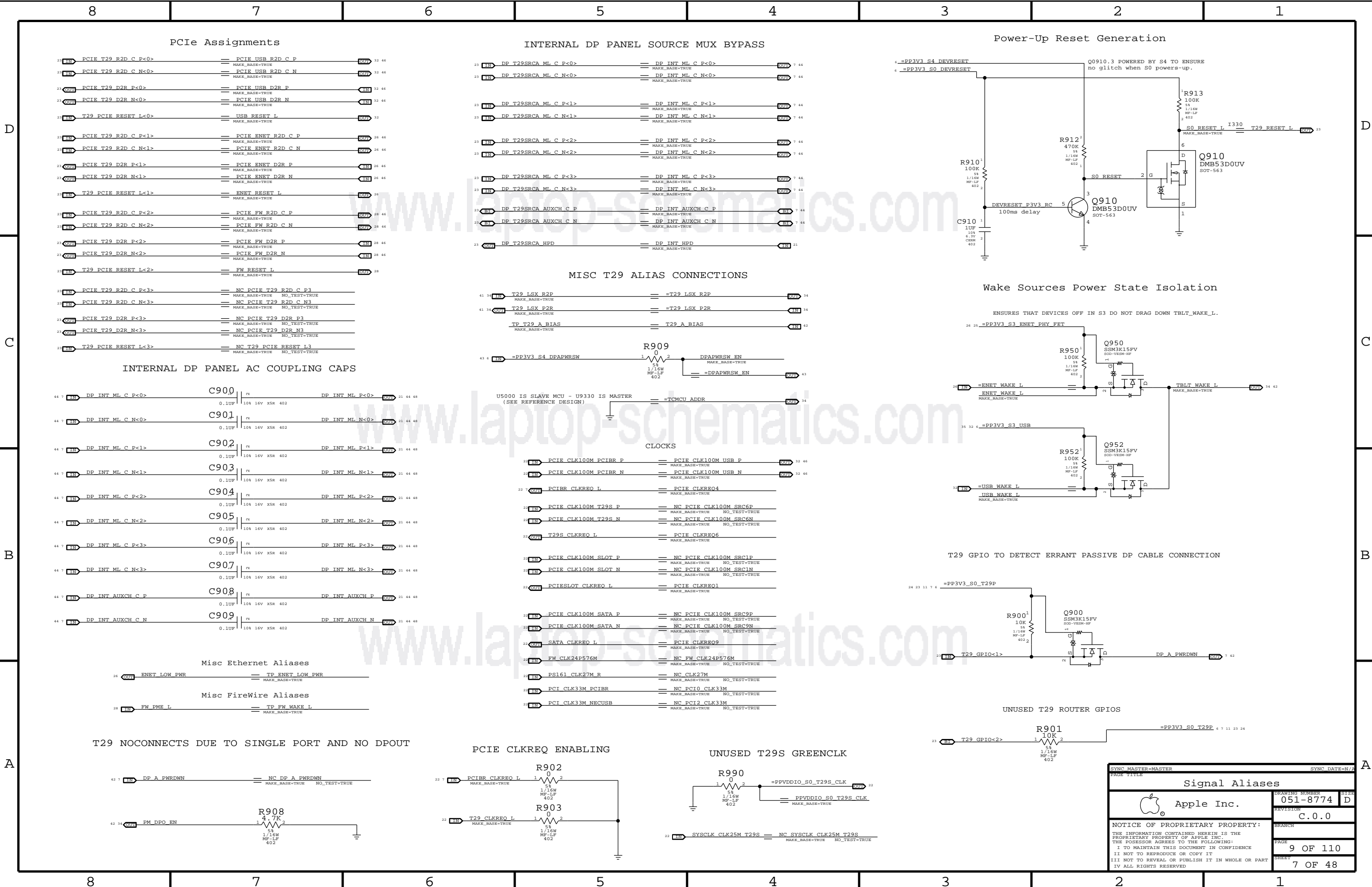
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		SHEET	2 OF 48

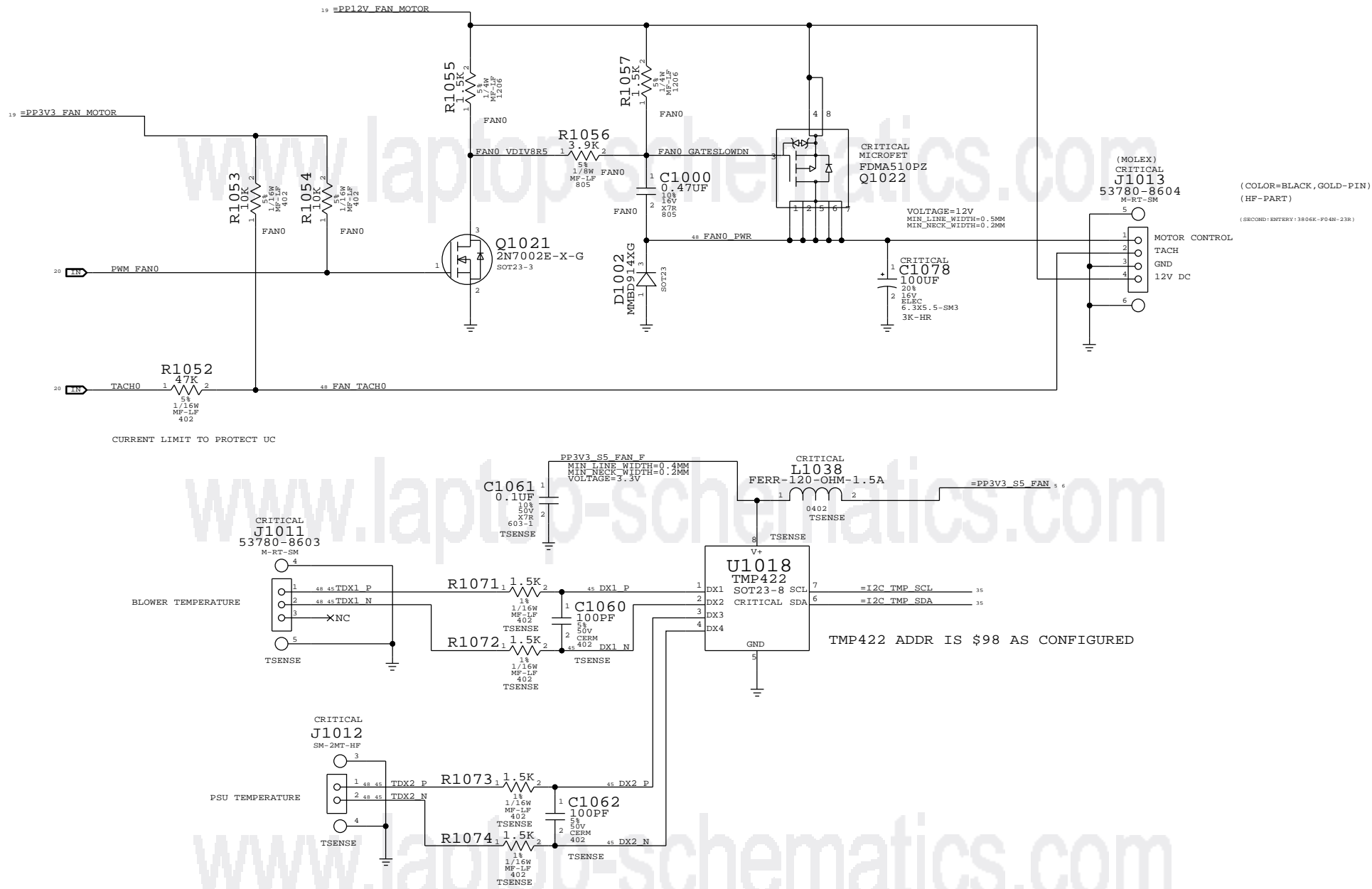







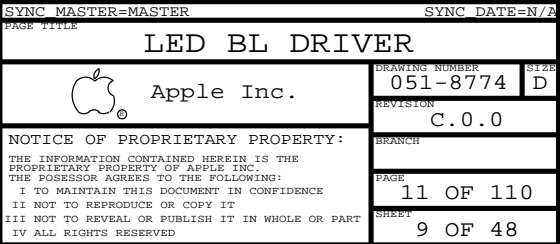






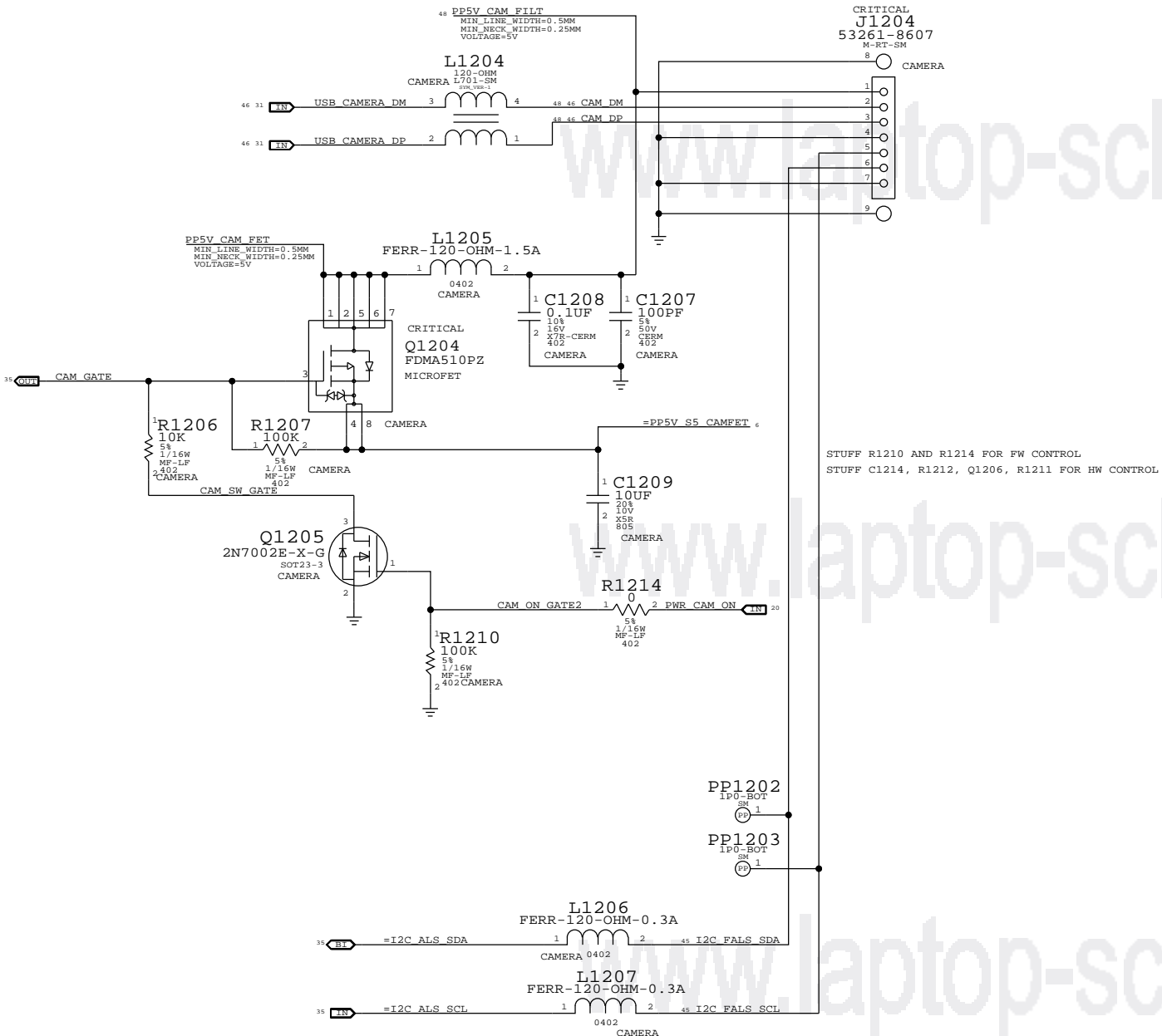
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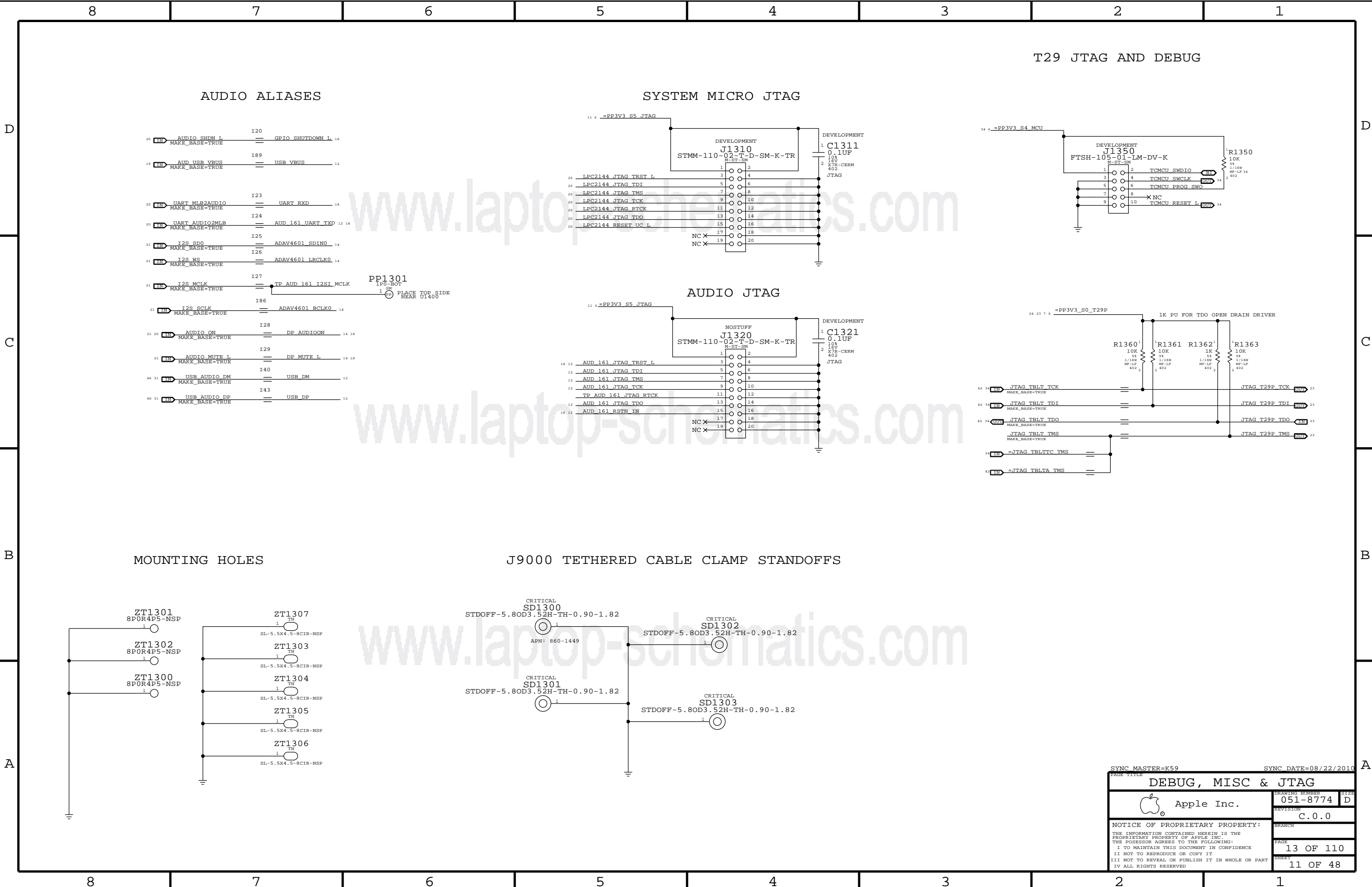


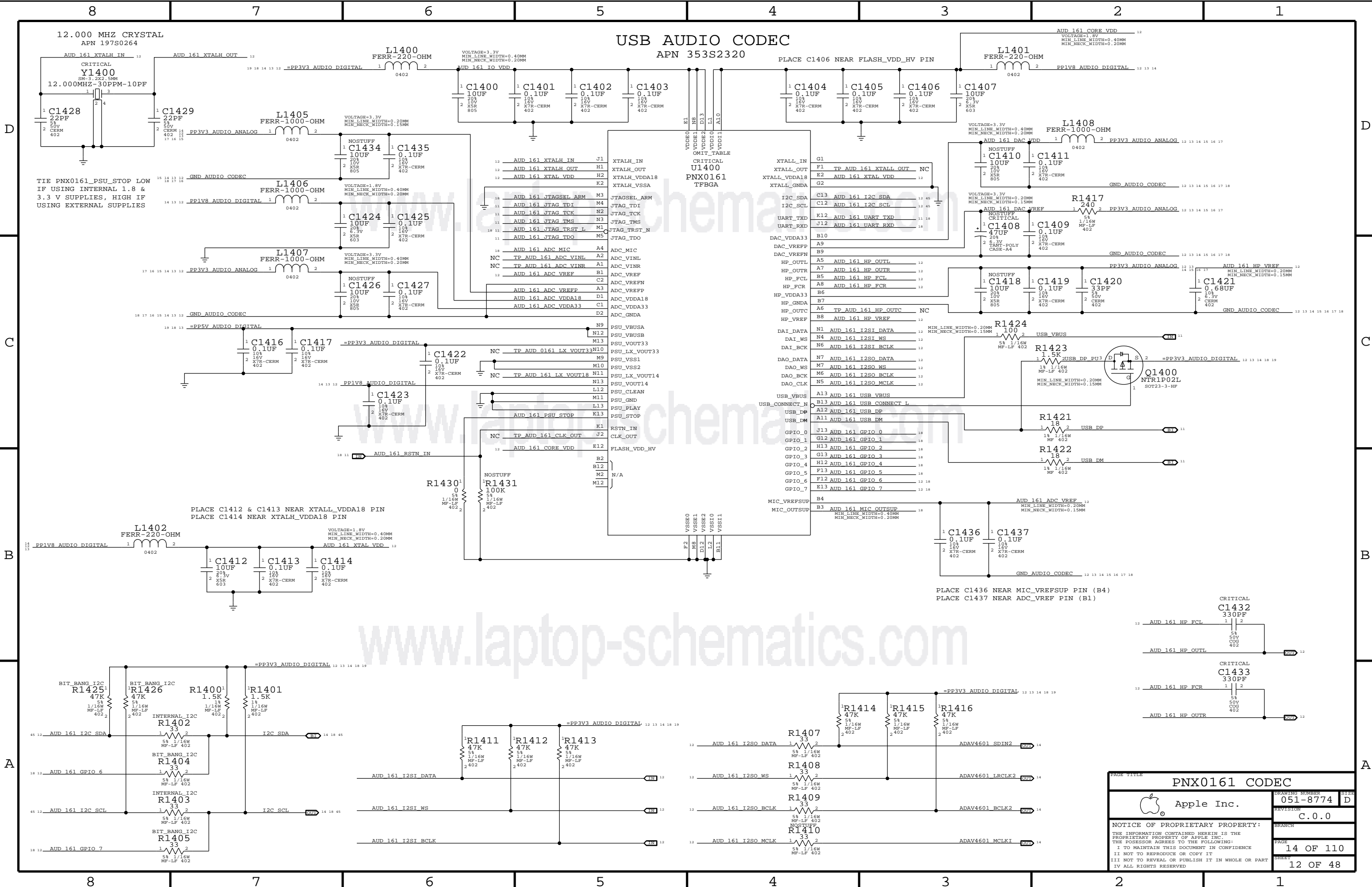
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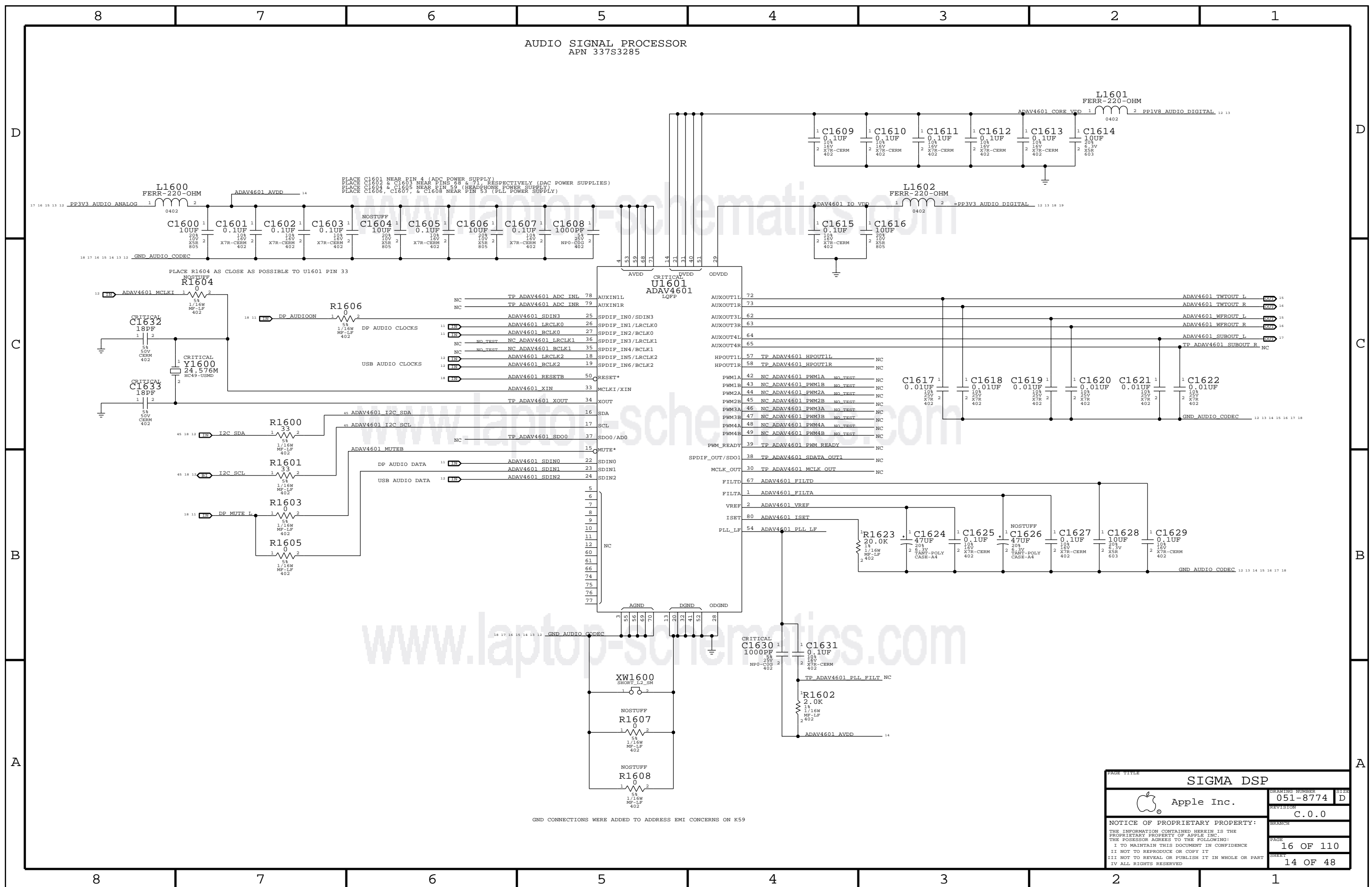
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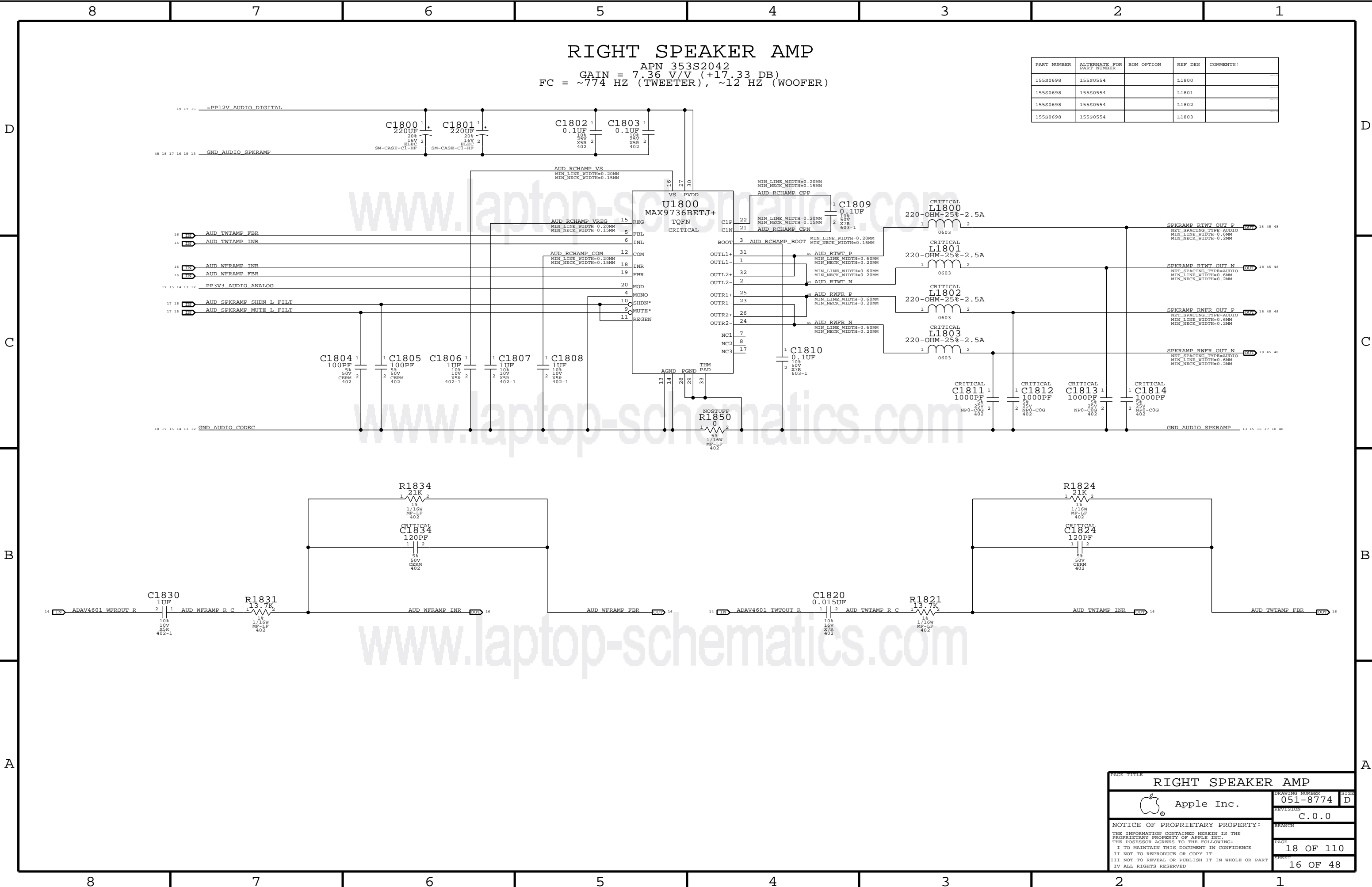






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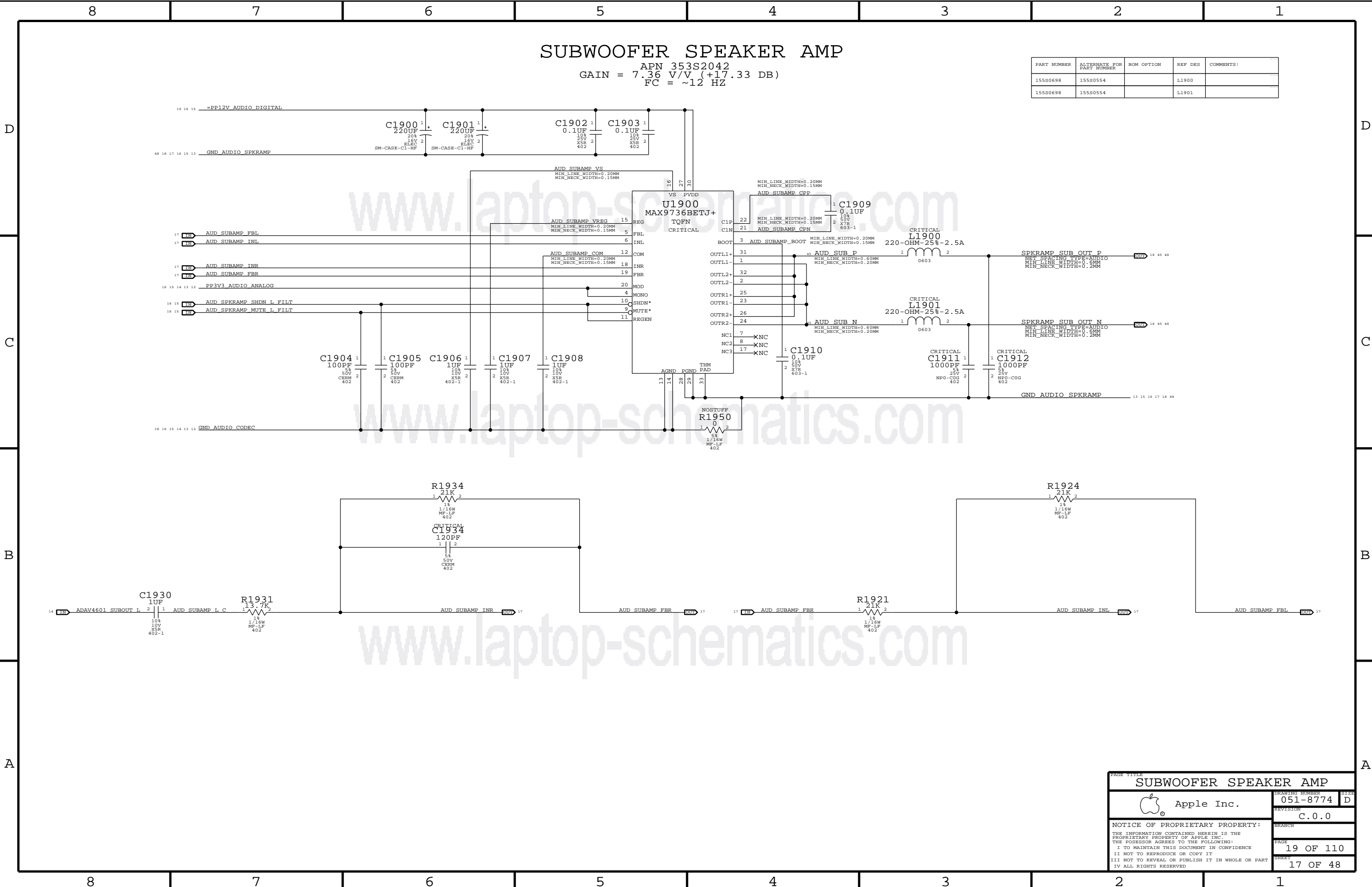
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0698	155S0554		L1800	
155S0698	155S0554		L1801	
155S0698	155S0554		L1802	
155S0698	155S0554		L1803	

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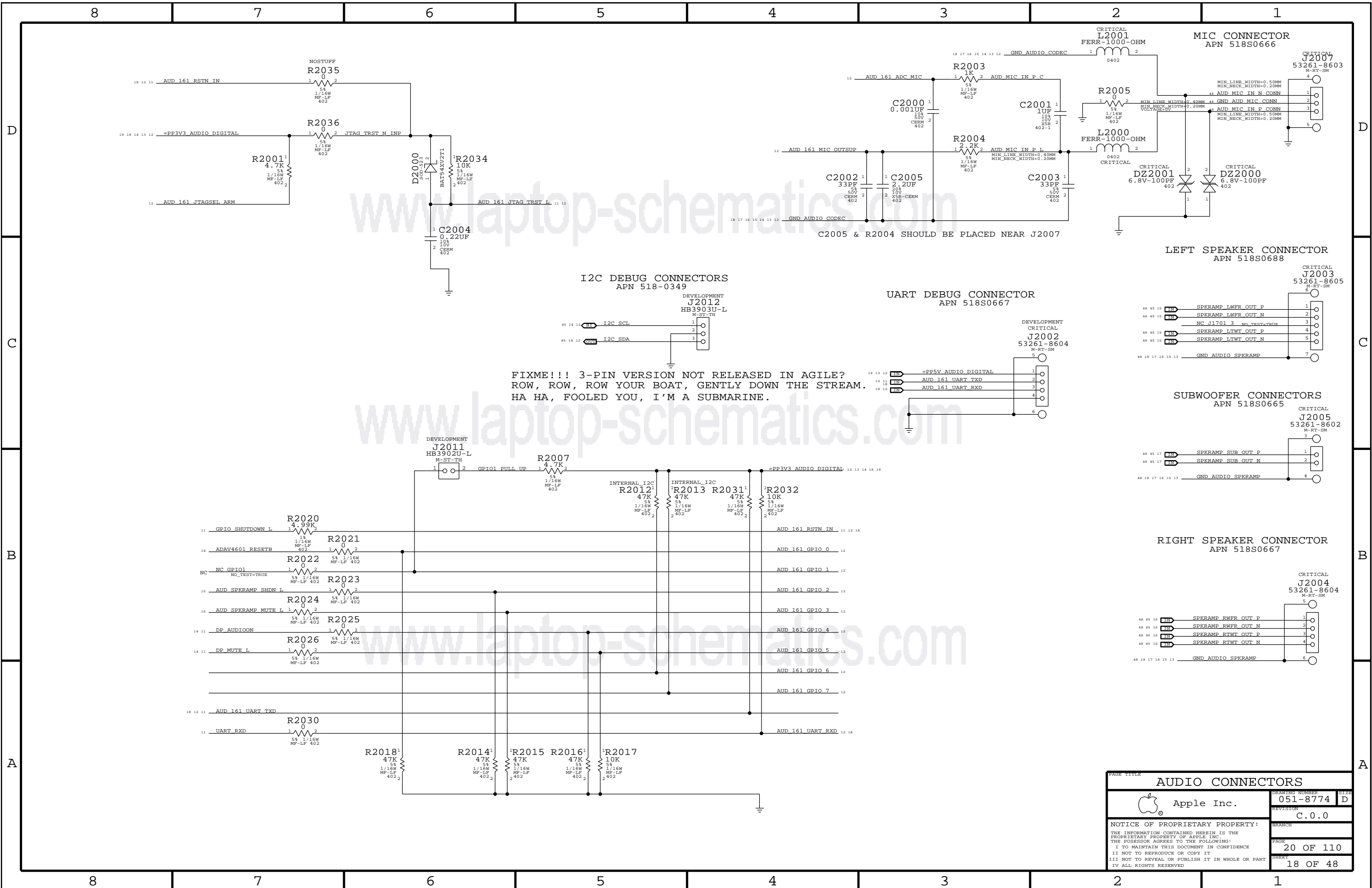





APN 353S2042  
GAIN = 7.36 V/V (+17.33 DB)  
FC = ~12 HZ

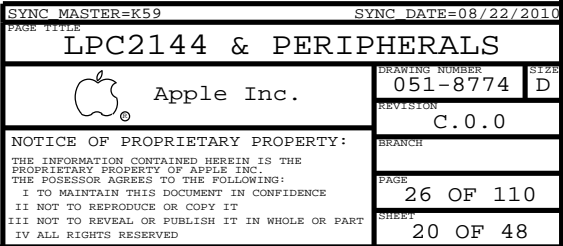
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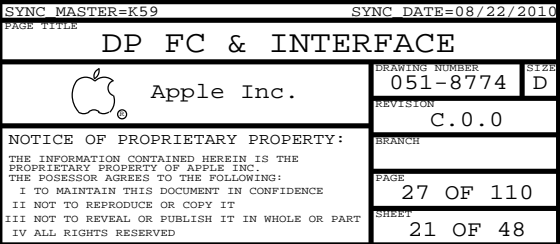
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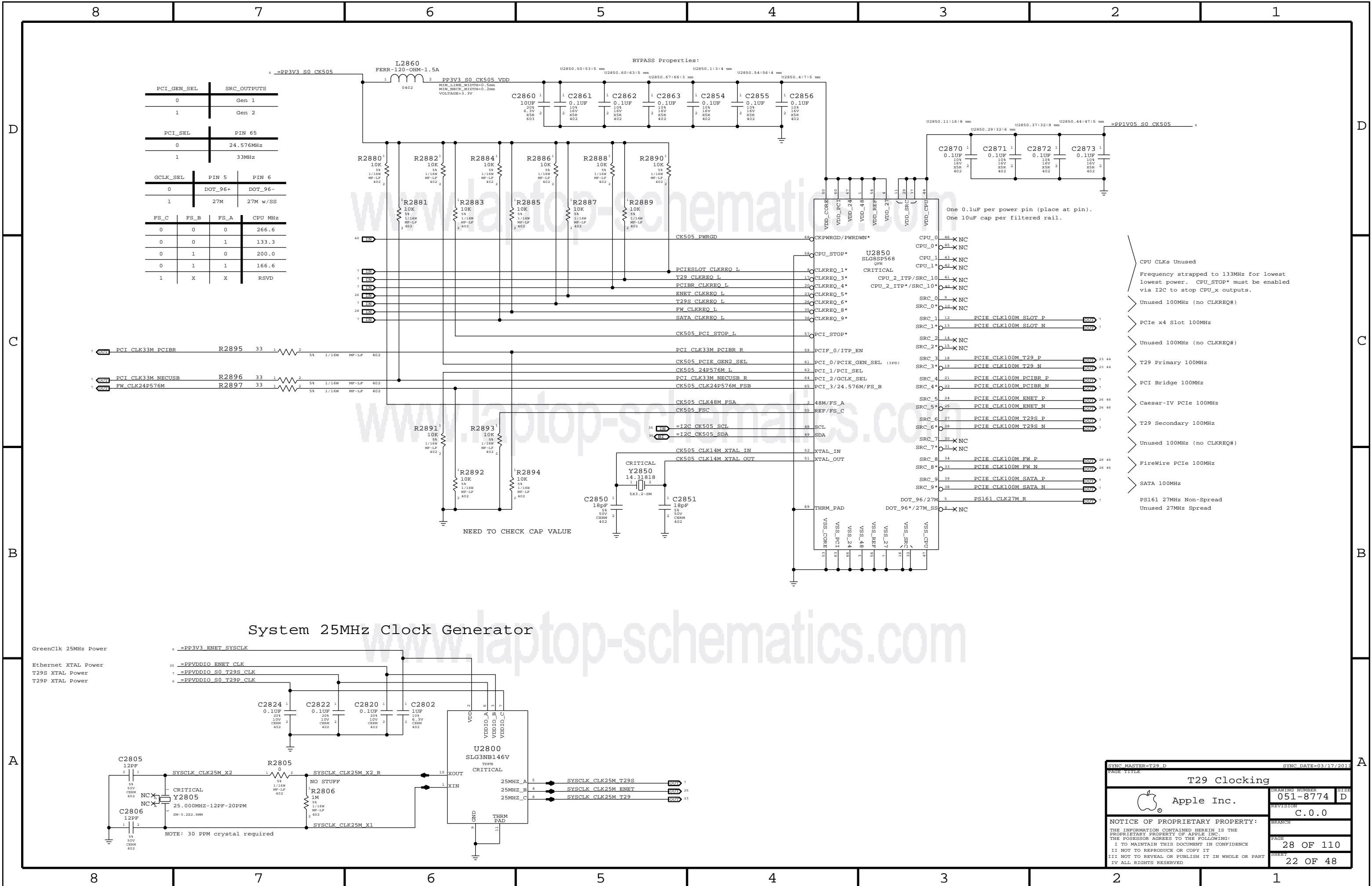
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AUDIO CONNECTORS		
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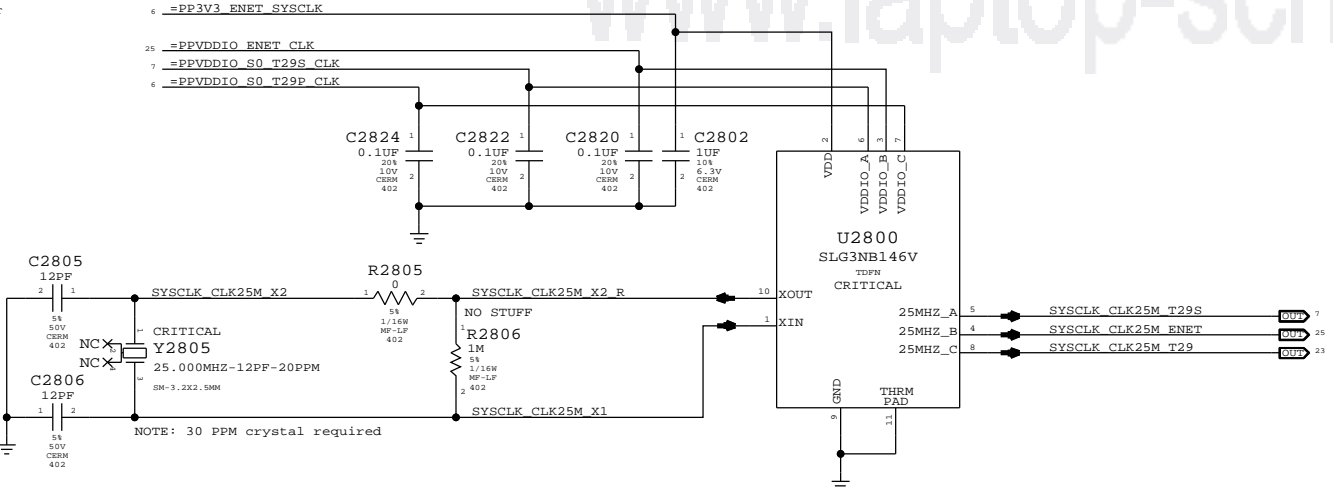


PCI_GEN_SEL		SRC_OUTPUTS	
0		Gen 1	
1		Gen 2	
PCI_SEL		PIN 65	
0		24.576MHz	
1		33MHz	
GCLK_SEL		PIN 5	PIN 6
0		DOT_96+	DOT_96-
1		27M	27M w/SS
FS_C	FS_B	FS_A	CPU MHz
0	0	0	266.6
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	X	X	RSVD

- CPU CLKs Unused
- Frequency strapped to 133MHz for lowest lowest power. CPU\_STOP\* must be enabled via I2C to stop CPU\_x outputs.
- Unused 100MHz (no CLKREQ#)
- PCIe x4 Slot 100MHz
- Unused 100MHz (no CLKREQ#)
- T29 Primary 100MHz
- PCI Bridge 100MHz
- Caesar-IV PCIe 100MHz
- T29 Secondary 100MHz
- Unused 100MHz (no CLKREQ#)
- FireWire PCIe 100MHz
- SATA 100MHz
- PS161 27MHz Non-Spread
- Unused 27MHz Spread

System 25MHz Clock Generator

GreenClk 25MHz Power  
Ethernet XTAL Power  
T29S XTAL Power  
T29P XTAL Power



SYNC MASTER=T29\_D

SYNC DATE=03/17/2013

T29 Clocking

Apple Inc.

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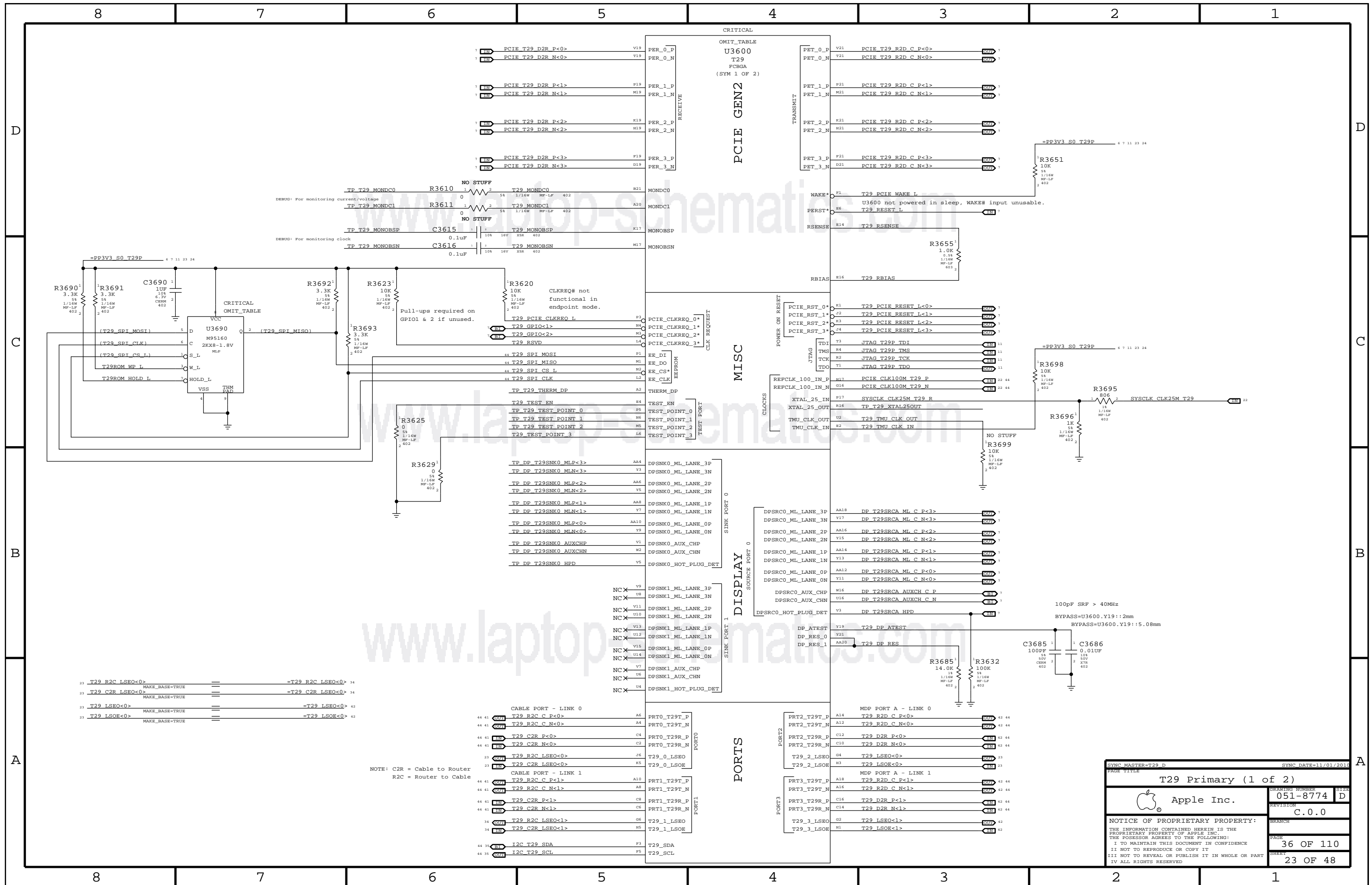
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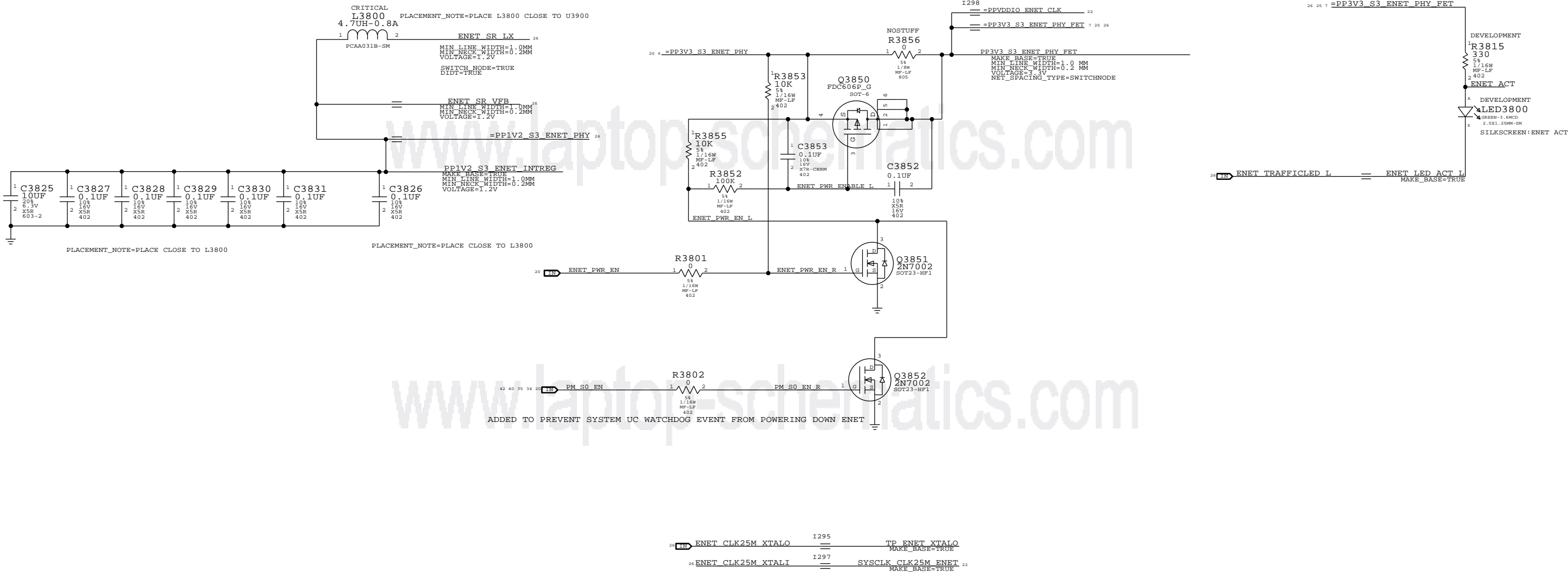





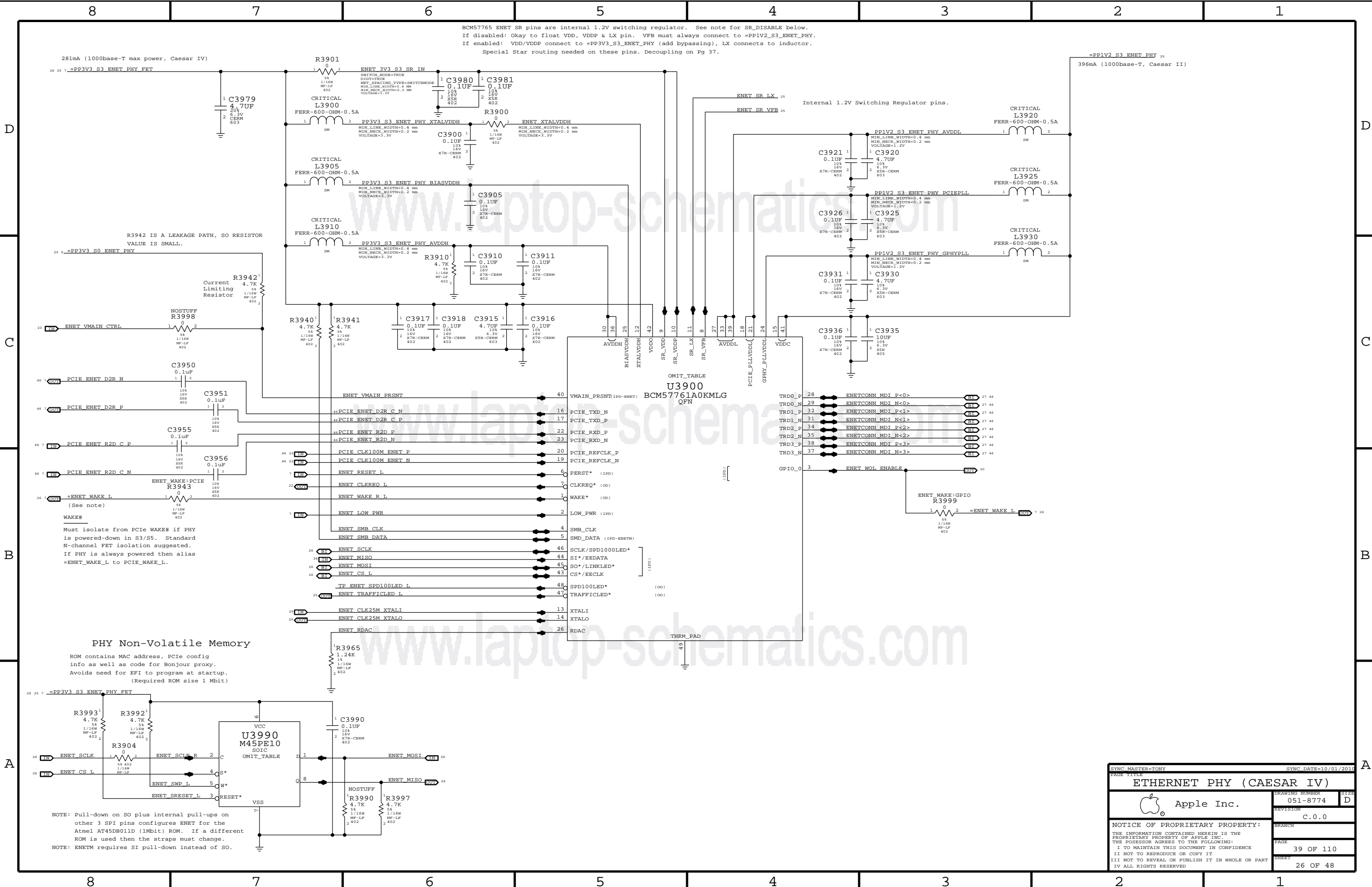
CAESAR IV 1.2V INT.VR CMPTS

CAESAR IV POWER ENABLE CIRCUIT

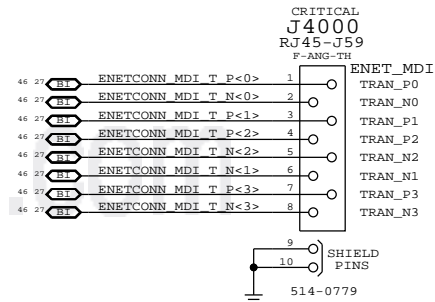
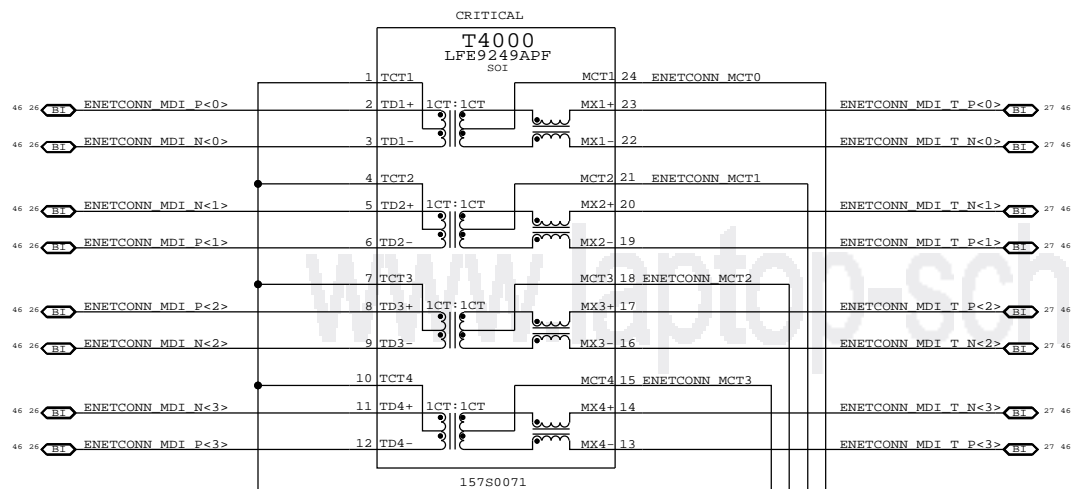
CAESAR IV ACTIVITY LED



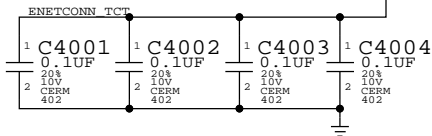
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CAESAR IV SUPPORT			
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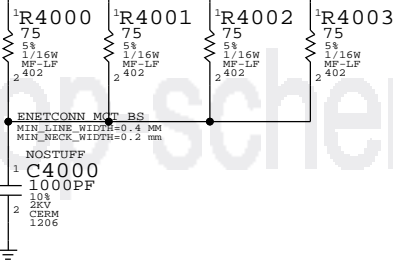
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PLACE C4001/2/3/4 CLOSE TO PINS 1/4/7/10 ON T4000!!!

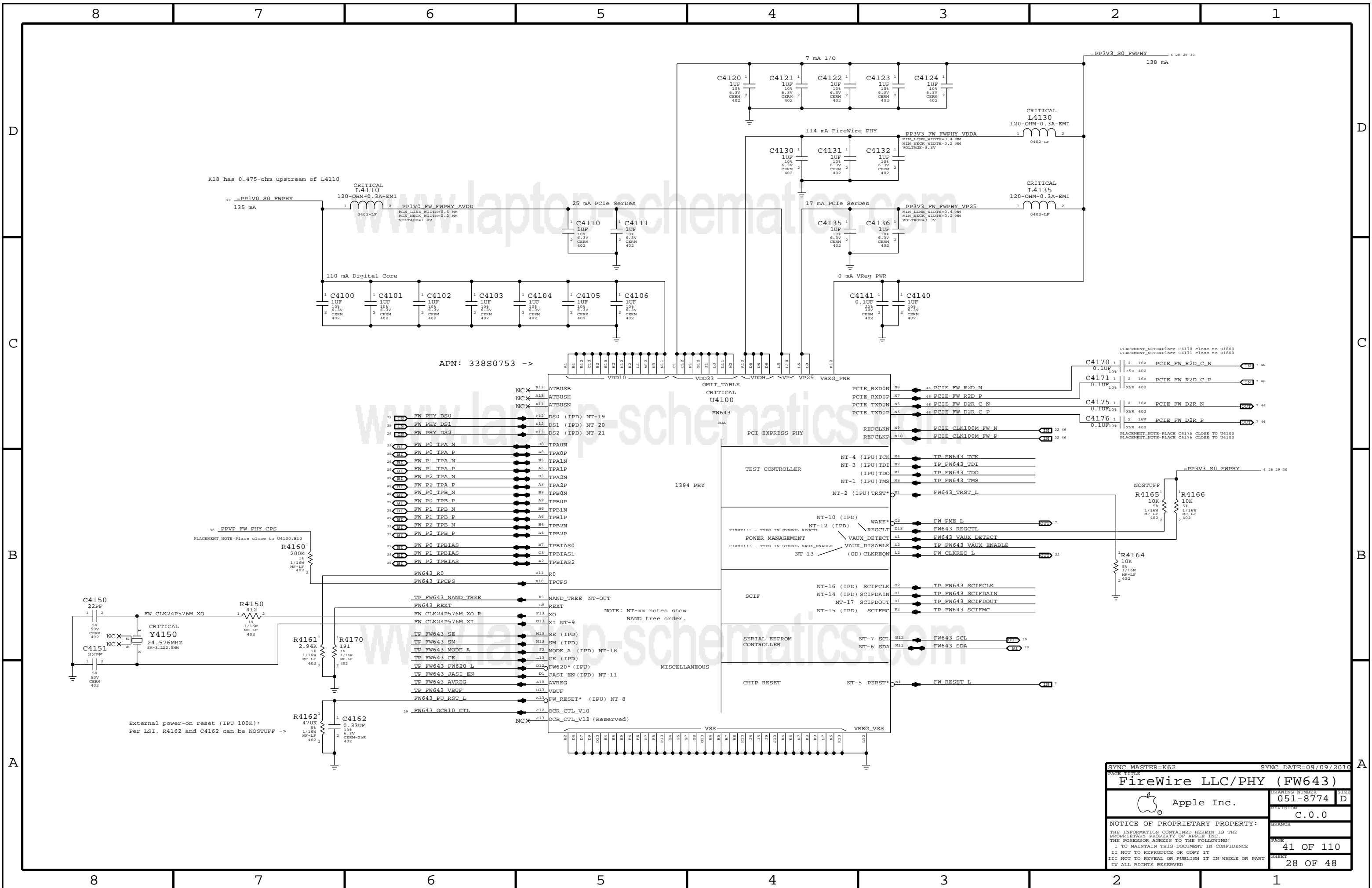


NOTE: Check with PHY and Magnetics MFR to determine what to do with center taps.

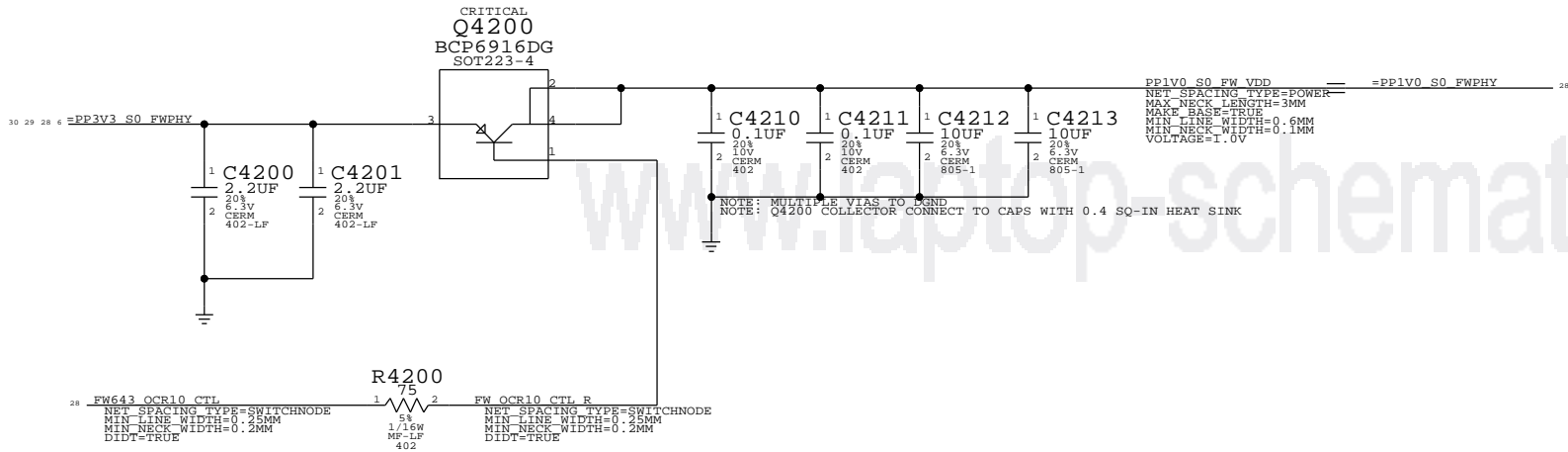


NOTE: BOB SMITH TERMINATION FOR EMC.

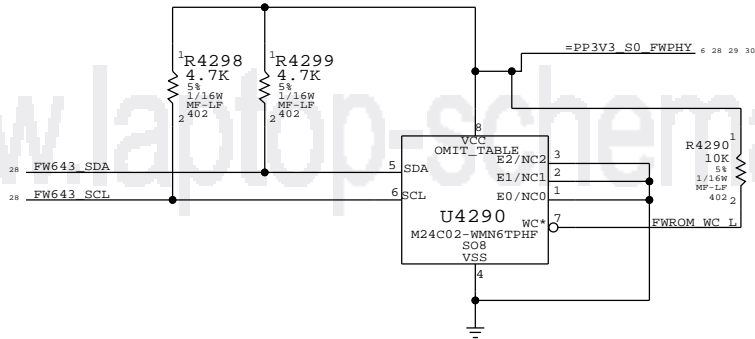
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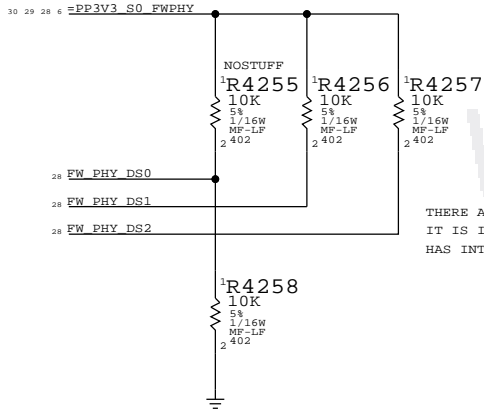
FW643 1.0V GENERATION



FW643 GUID ROM

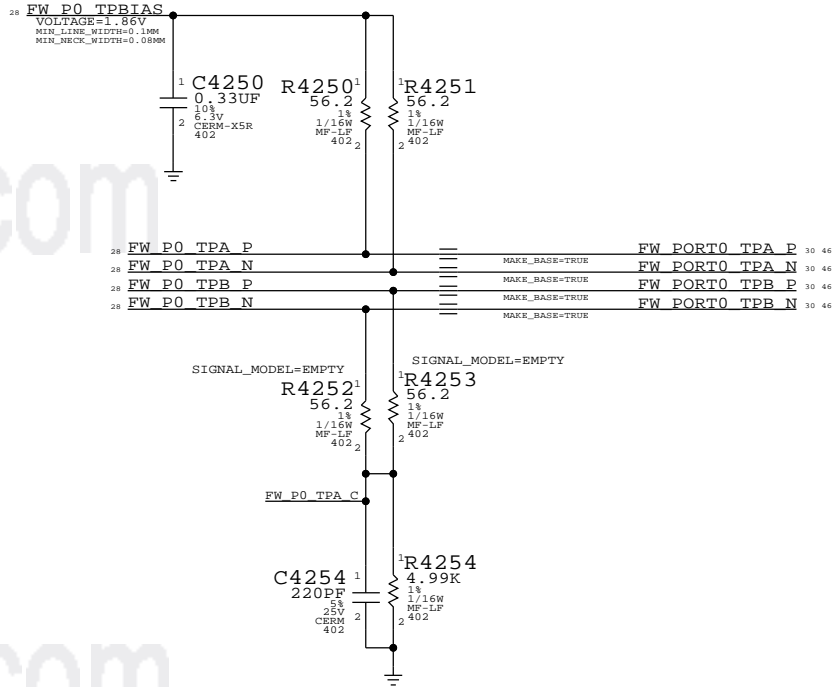


1394 PHY DATA/STROBE OPTIONS



THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED. NO STUFF MEANS THAT IT IS IN BILINGUAL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE, FW643 HAS INTERNAL 100K PULL-DOWNS, ONLY PULL-UPS NECESSARY.

Termination  
Place close to FireWire PHY




2ND & 3RD TPA/TPB PAIR UNUSED

FW_P1_TPBias	=	NC FW_PORT1_TPBias
FW_P1_TPA_P	=	NC FW_PORT1_TPA_P
FW_P1_TPA_N	=	NC FW_PORT1_TPA_N
FW_P1_TPB_P	=	NC FW_PORT1_TPB_P
FW_P1_TPB_N	=	NC FW_PORT1_TPB_N
FW_P2_TPBias	=	NC FW_PORT2_TPBias
FW_P2_TPA_P	=	NC FW_PORT2_TPA_P
FW_P2_TPA_N	=	NC FW_PORT2_TPA_N
FW_P2_TPB_P	=	NC FW_PORT2_TPB_P
FW_P2_TPB_N	=	NC FW_PORT2_TPB_N

NOTE: AGERE'S RECOMMENDATION FOR UNUSED PORTS


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FireWire: 1394B MISC			
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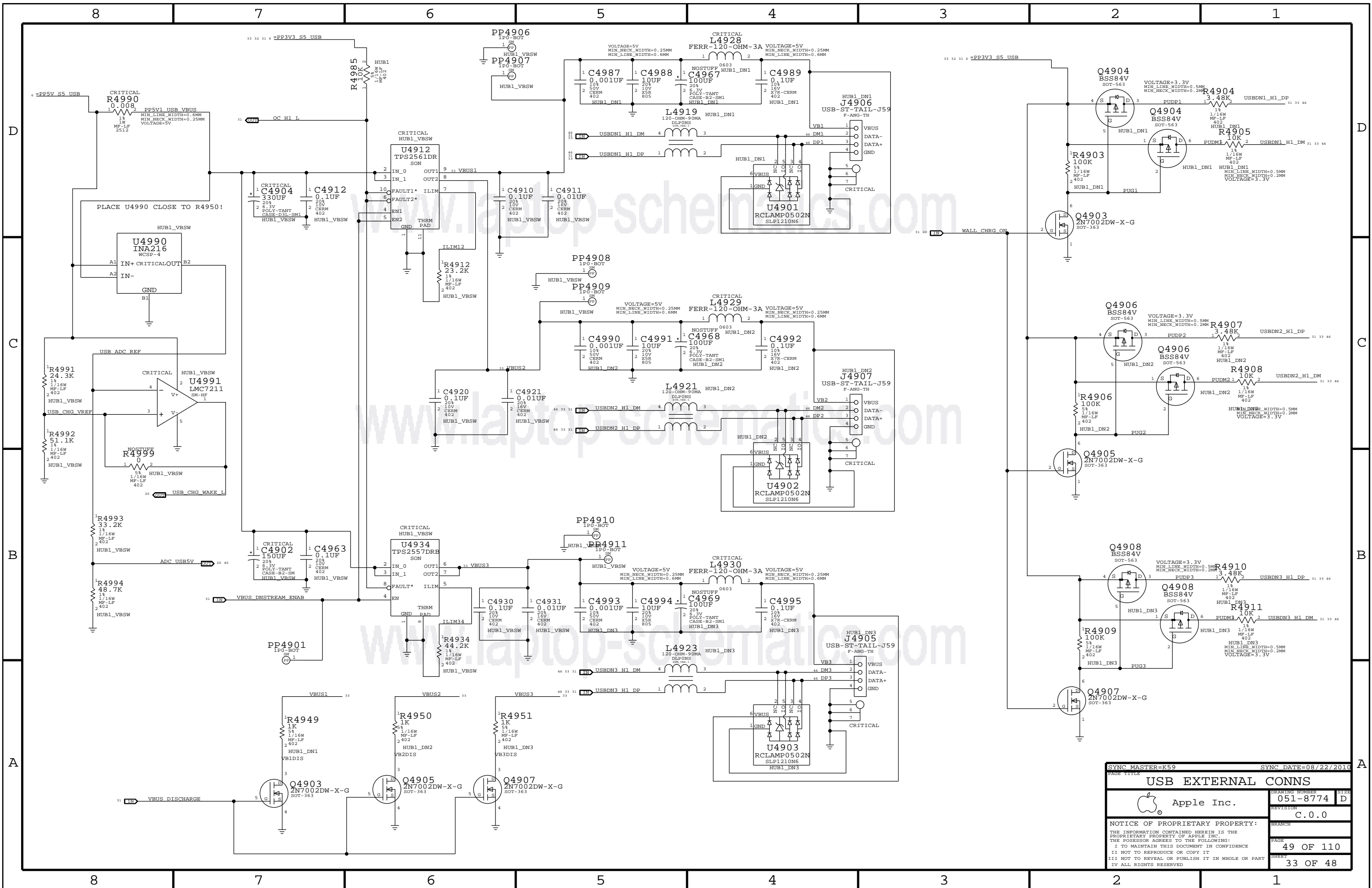





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USB 7-PORT HUB			
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USB EXTERNAL CONNS			
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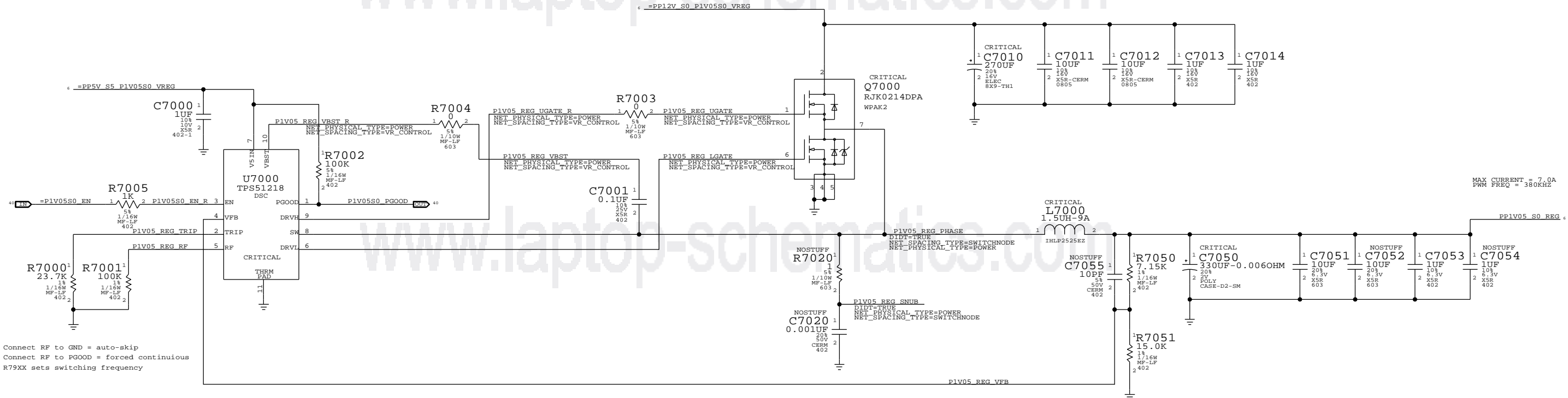
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
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Power aliases required by this page:

- PVPIN\_SW\_T29BST (8-13V Boost Input)
- PPl5V\_T29\_REG (15V Boost Output)


Signal aliases required by this page:

(NONE)

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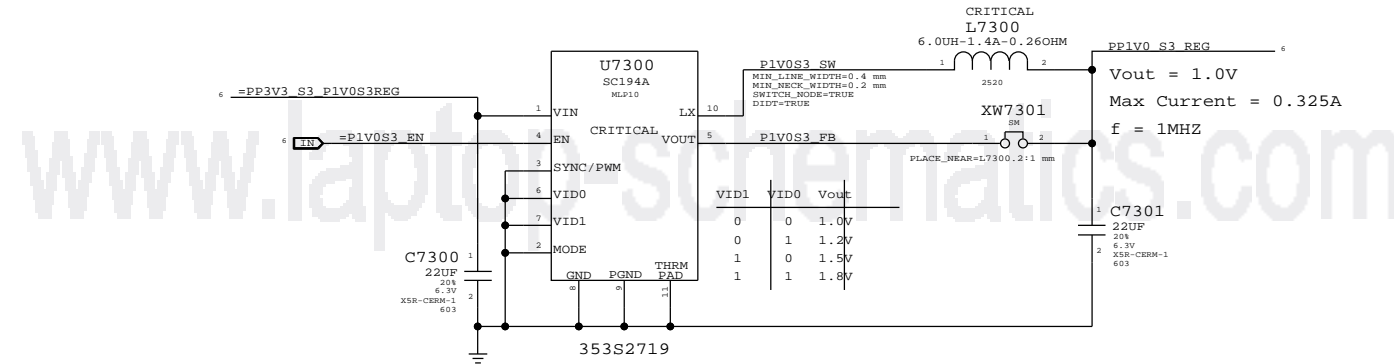
BOM options provided by this page:

T29BST - Stuffs 15V boost regulator

SYNC MASTER-T29 D		SYNC DATE-03/17/2011	
PAGE TITLE			
Power: T29 15V Boost			
 Apple Inc.		DRAWING NUMBER	SIZE
		051-8774	D
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		C. 0.0	
		BRANCH	
		PAGE	71 OF 110
		SHEET	37 OF 48

www.laptop-schematics.com

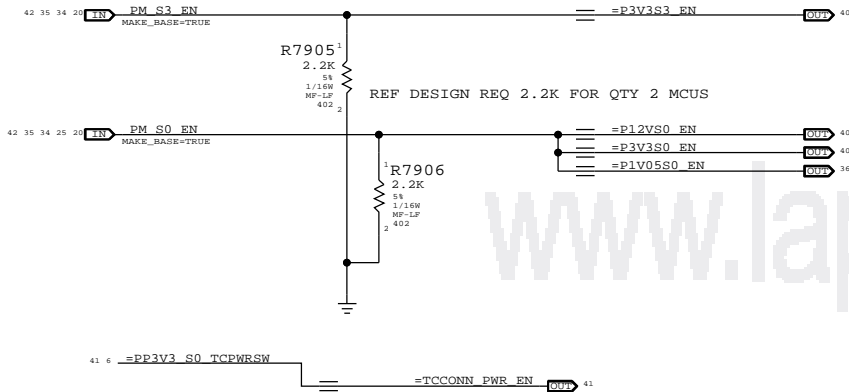
1.0V Switcher



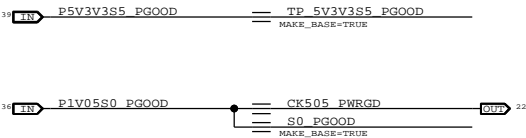
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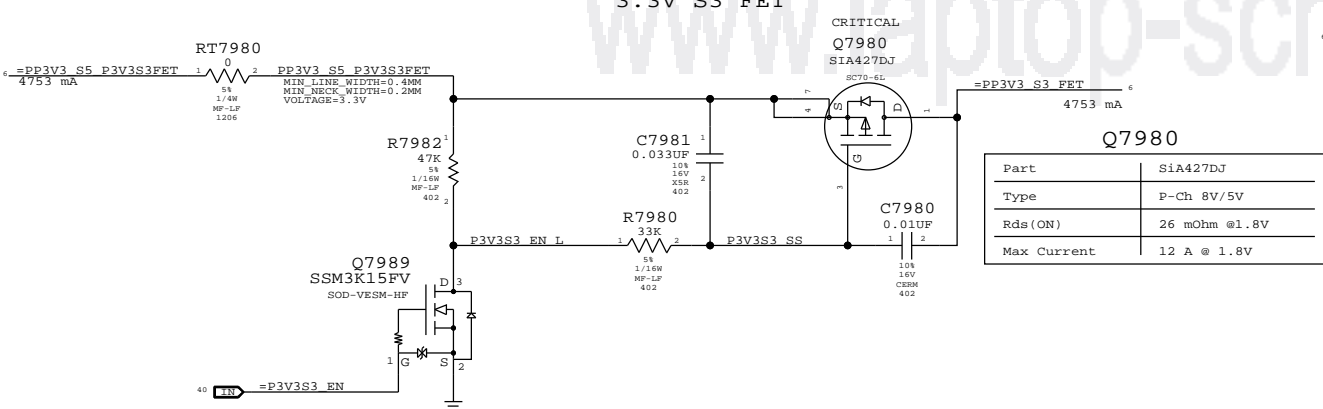
T29 / Device Rails



Power Goods

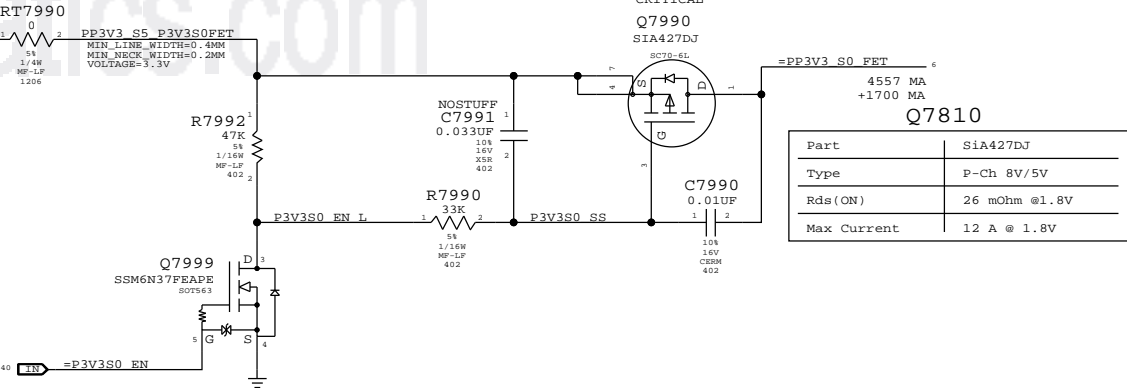


3.3V S3 FET



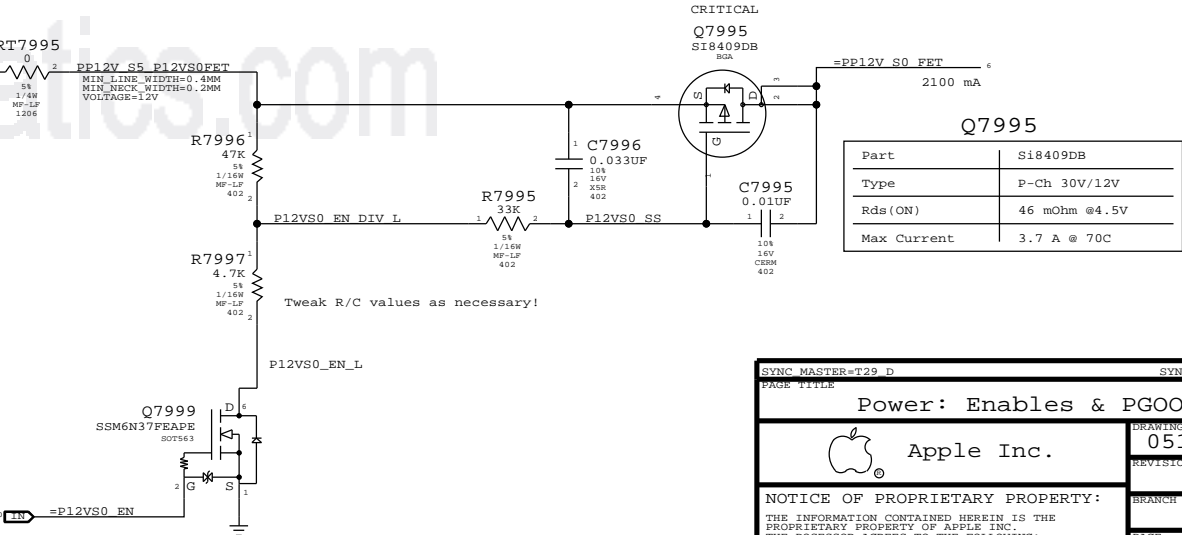
Part	SiA427DJ
Type	P-Ch 8V/5V
Rds(ON)	26 mOhm @1.8V
Max Current	12 A @ 1.8V

3.3V S0 FET



Part	SiA427DJ
Type	P-Ch 8V/5V
Rds(ON)	26 mOhm @1.8V
Max Current	12 A @ 1.8V

12V S0 FET



Part	Si8409DB
Type	P-Ch 30V/12V
Rds(ON)	46 mOhm @4.5V
Max Current	3.7 A @ 70C

SYNC MASTER=T29\_D

SYNC DATE=09/30/2010

Power: Enables & PGOODS

Apple Inc.

051-8774

051-8774

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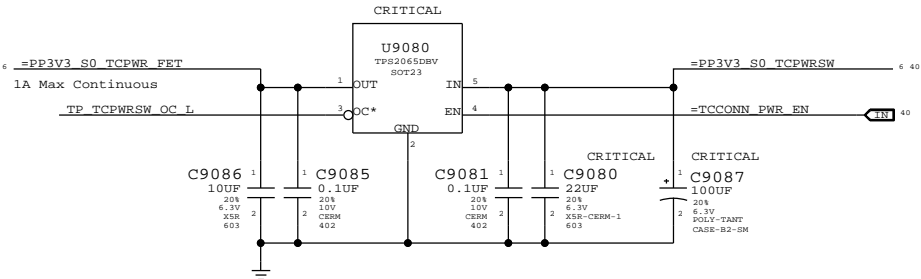
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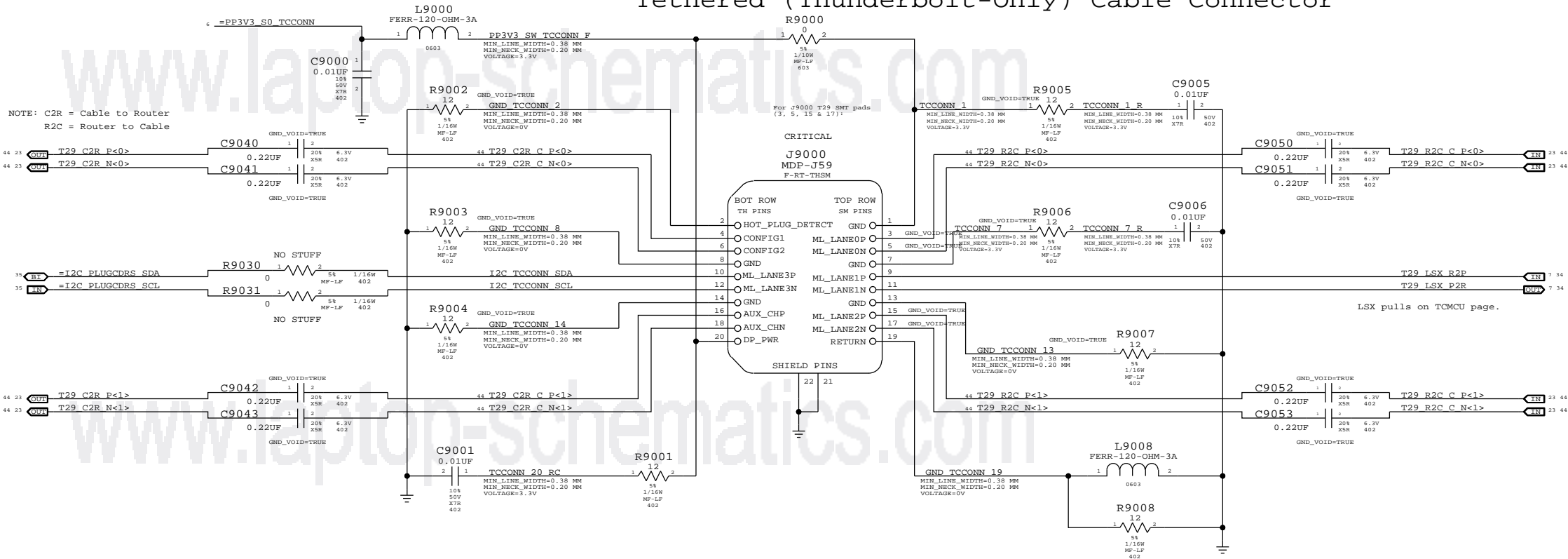
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
A

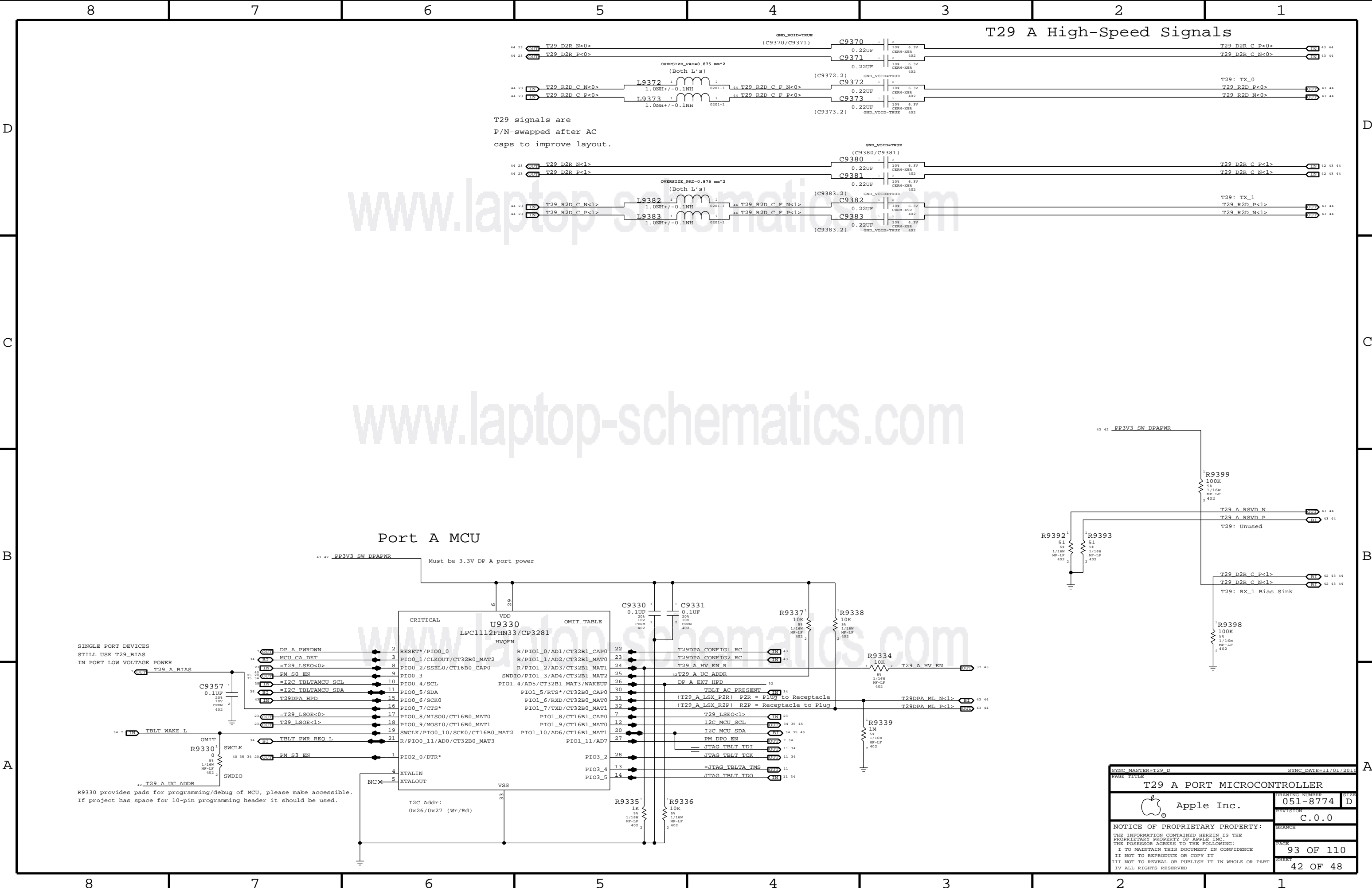
Cable 3.3V Power Switch



Tethered (Thunderbolt-Only) Cable Connector



SYNC MASTER=T29 D		SYNC DATE=03/17/2013	
PAGE TITLE			
Tethered Cable Connector		DRAWING NUMBER	051-8774
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SYNC MASTER=T29 D		SYNC DATE=11/01/2010	
PAGE TITLE		T29 A PORT MICROCONTROLLER	
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3.3V/HV Power MUX

Port A 3.3V Power Switch

Port A HV Power Switch

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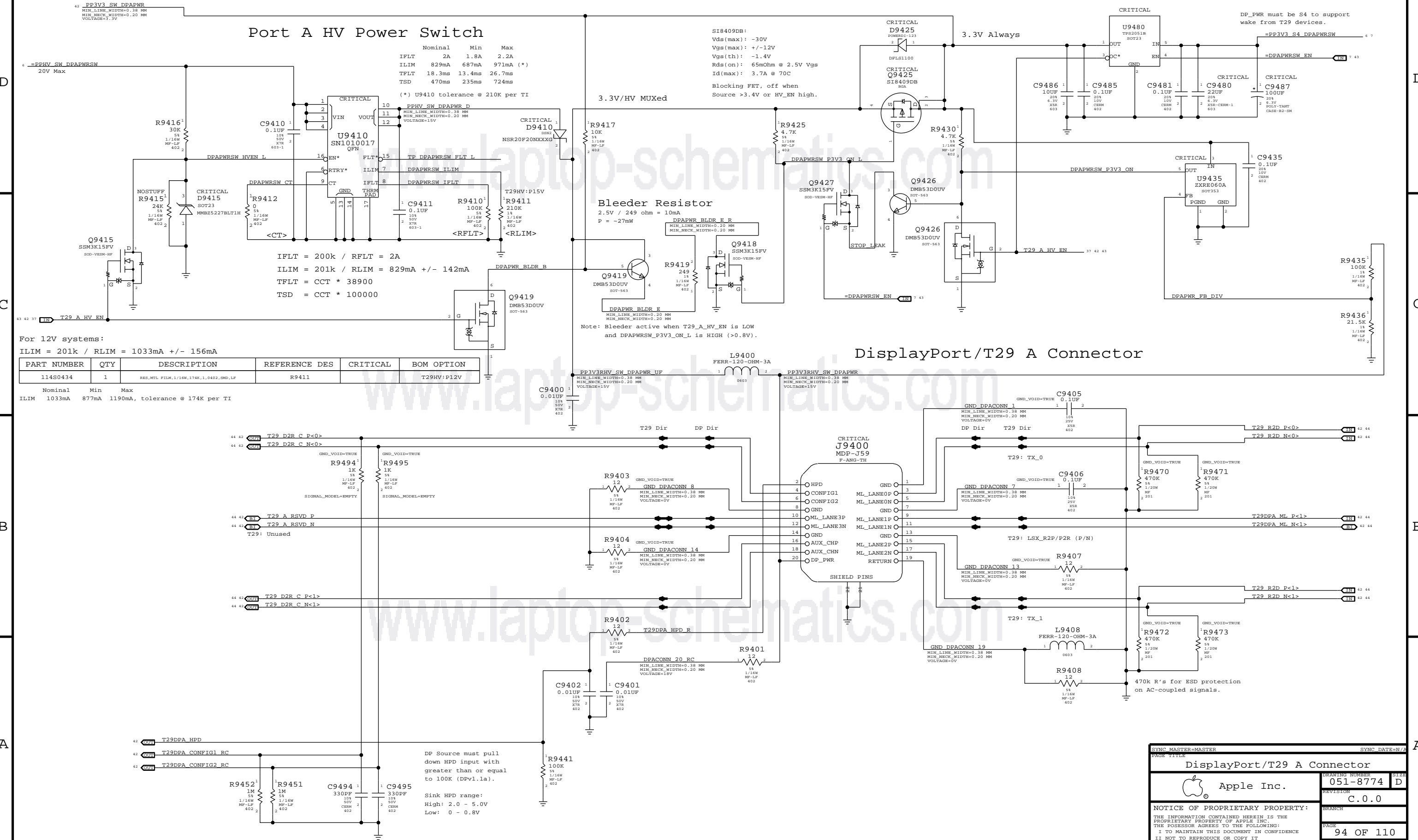
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SYNC MASTER=MASTER		SYNC DATE=N/A	
PAGE TITLE			
DisplayPort/T29 A Connector		Drawing	
 Apple Inc.		DRAWING NUMBER	SHEET
		051-8774	D
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		PAGE	94 OF 110
		SHEET	43 OF 48

## PCI-Express Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
PCIEG2_85D	*	N	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
PCIEG2_85D	TOP_BOTTOM	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
PCIEG2	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP, BOTTOM	=4X_DIELECTRIC	?
PCIEG2	TOP, BOTTOM	=4X_DIELECTRIC	?

## T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
I2C_55SE	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	0_1MM	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
I2C	*	=2x_DIELECTRIC	?

## T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

## T29/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_90D	*	N	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
T29DP_90D	TOP,BOTTOM	Y	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

## DP CONNECTOR SIGNAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=4:1_SPACING	?


SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4:1_SPACING	?

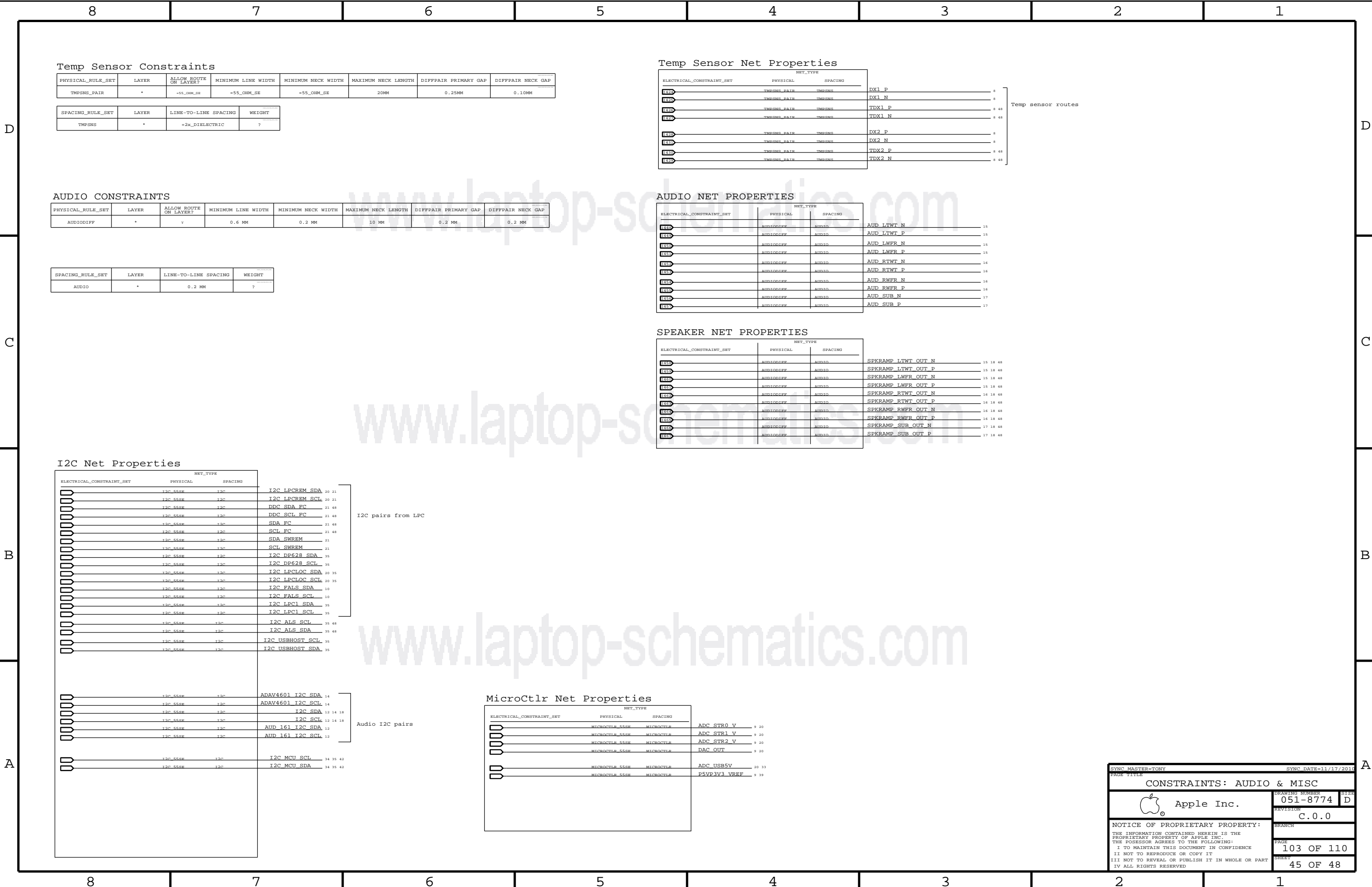
## T29 Net Properties

ELECTRICAL CONSTRAINT SET		NET TYPE		
		PHYSICAL	SPACING	
	PCIE_CLK100M_T29	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_P 23 23
	PCIE_CLK100M_T29	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_N 23 23
		T29_55SE	T29C	I2C_T29_SCL 23 35
		T29_55SE	T29C	I2C_T29_SDA 23 35
	T29_SPT_CLK	T29_SPT_55S	T29_SPT	T29_SPI_CLK 23
	T29_SPT_MOSI	T29_SPT_55S	T29_SPT	T29_SPI_MOSI 23
	T29_SPT_MISO	T29_SPT_55S	T29_SPT	T29_SPI_MISO 23
	T29_SPT_CS_L	T29_SPT_55S	T29_SPT	T29_SPI_CS_L 23
		T29DP_90D	T29DP	T29_R2D_C_P<3..0> 23 42
		T29DP_90D	T29DP	T29_R2D_C_N<3..0> READ_PROBE=TRUE 23 42
		T29DP_90D	T29DP	T29_D2R_P<3..0> READ_PROBE=TRUE 23 42
		T29DP_90D	T29DP	T29_D2R_N<3..0> READ_PROBE=TRUE 23 42
	T29_R2D0	T29DP_90D	T29DP	T29_R2D_P<0> 42 43
	T29_R2D0	T29DP_90D	T29DP	T29_R2D_N<0> READ_PROBE=TRUE 42 43
	T29_R2D1	T29DP_90D	T29DP	T29_R2D_P<1> READ_PROBE=TRUE 42 43
	T29_R2D1	T29DP_90D	T29DP	T29_R2D_N<1> READ_PROBE=TRUE 42 43
		T29DP_90D	T29DP	T29_R2D_C_F_P<1..0> 42
		T29DP_90D	T29DP	T29_R2D_C_F_N<1..0> READ_PROBE=TRUE 42
	T29_D2R0	T29DP_90D	T29DP	T29_D2R_C_P<0> 42 43
	T29_D2R0	T29DP_90D	T29DP	T29_D2R_C_N<0> READ_PROBE=TRUE 42 43
	T29_D2R1	T29DP_90D	T29DP	T29_D2R_C_P<1> READ_PROBE=TRUE 42 43
	T29_D2R1	T29DP_90D	T29DP	T29_D2R_C_N<1> READ_PROBE=TRUE 42 43
	DP_90D	DISPLAYPORT		T29DPA_ML_P<1> 42 43
	DP_90D	DISPLAYPORT		T29DPA_ML_N<1> 42 43
	USB2_90D	USB2		T29_A_RSVD_P 42 43
	USB2_90D	USB2		T29_A_RSVD_N 42 43
		T29DP_90D	T29DP	T29_R2C_P<1..0> 41
		T29DP_90D	T29DP	T29_R2C_N<1..0> READ_PROBE=TRUE 41
	T29_R2C0	T29DP_90D	T29DP	T29_R2C_C_P<0> 23 41
	T29_R2C0	T29DP_90D	T29DP	T29_R2C_C_N<0> READ_PROBE=TRUE 23 41
	T29_R2C1	T29DP_90D	T29DP	T29_R2C_C_P<1> READ_PROBE=TRUE 23 41
	T29_R2C1	T29DP_90D	T29DP	T29_R2C_C_N<1> READ_PROBE=TRUE 23 41
	T29_C2R0	T29DP_90D	T29DP	T29_C2R_P<0> READ_PROBE=TRUE 23 41
	T29_C2R0	T29DP_90D	T29DP	T29_C2R_N<0> 23 41
	T29_C2R1	T29DP_90D	T29DP	T29_C2R_P<1> READ_PROBE=TRUE 23 41
	T29_C2R1	T29DP_90D	T29DP	T29_C2R_N<1> 23 41
		T29DP_90D	T29DP	T29_C2R_C_P<1..0> 41
		T29DP_90D	T29DP	T29_C2R_C_N<1..0> READ_PROBE=TRUE 41

## INTERNAL PANEL PROPERTIES

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
DE50	DE_50D	DISPLAYPORT	DP INT ML C P<3..0>
DE59	DE_50D	DISPLAYPORT	DP INT ML C N<3..0>
DE60	DE_50D	DISPLAYPORT	DP INT ML P<3..0>
DE65	DE_50D	DISPLAYPORT	DP INT ML N<3..0>
DE66	DE_50D	DISPLAYPORT	DP INT AUXCH C P
DE68	DE_50D	DISPLAYPORT	DP INT AUXCH C N
DE72	DE_50D	DISPLAYPORT	DP INT AUXCH P
DE89	DE_50D	DISPLAYPORT	DP INT AUXCH N

SYNC MASTER=TONY		SYNC DATE=11/17/2010	
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CONSTRAINTS: T29			
	Apple Inc.	DRAWING NUMBER	051-8774
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## Ethernet MDI Constraints

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001\_v01), Section 2.7.4

## PCIe Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
<b>SD00</b>	PCI_E_SSD	PCI_E	PCI_E ENET R2D P 26
<b>SD00</b>	PCI_E_SSD	PCI_E	PCI_E ENET R2D N 26
<b>SD00</b>	PCI_E_ENET_R2D	PCI_E	PCI_E ENET R2D C P 7 26
<b>SD00</b>	PCI_E_ENET_R2D	PCI_E	PCI_E ENET R2D C N 7 26
<b>SD00</b>	PCI_E_ENET_D2R	PCI_E	PCI_E ENET D2R P 7 26
<b>SD00</b>	PCI_E_ENET_D2R	PCI_E	PCI_E ENET D2R N 7 26
<b>SD00</b>	PCI_E_SSD	PCI_E	PCI_E ENET D2R C P 26
<b>SD00</b>	PCI_E_SSD	PCI_E	PCI_E ENET D2R C N 26
<b>SD00</b>	CLK_CLK100M_ENET	CLK_PCI_E	PCI_E CLK100M ENET P 22 26
<b>SD00</b>	CLK_CLK100M_ENET	CLK_PCI_E	PCI_E CLK100M ENET N 22 26

## FireWire Interface Constraints

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

## FIREWIRE PCIE NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
		PCIE_R5D	PCIE	PCIE_FW_R2D_P	28
		PCIE_R5D	PCIE	PCIE_FW_R2D_N	28
	PCIE_FW_R2D	PCIE_R5D	PCIE	PCIE_FW_R2D_C_P	7 28
	PCIE_FW_R2D	PCIE_R5D	PCIE	PCIE_FW_R2D_C_N	7 28
	PCIE_FW_D2R	PCIE_R5D	PCIE	PCIE_FW_D2R_P	7 28
	PCIE_FW_D2R	PCIE_R5D	PCIE	PCIE_FW_D2R_N	7 28
	PCIE_FW_D2R	PCIE_R5D	PCIE	PCIE_FW_D2R_C_P	7 28
	PCIE_FW_D2R	PCIE_R5D	PCIE	PCIE_FW_D2R_C_N	7 28
	PCIE_CLK100M_FW	CLK_PCIE_40D	CLK_PCIE	PCIE_CLK100M_FW_P	22 28
	PCIE_CLK100M_FW	CLK_PCIE_40D	CLK_PCIE	PCIE_CLK100M_FW_N	22 28

## USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB2_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2	*	=4:1_SPACING	?





## USB PCIE NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
	PCIEQ2_85D	PCIEQ2	PCIE USB D2R C P
	PCIEQ2_85D	PCIEQ2	PCIE USB D2R C N
	PCIEQ2_85D	PCIEQ2	PCIE USB R2D P
	PCIEQ2_85D	PCIEQ2	PCIE USB R2D N
PCIE_USB_R2D	PCIEQ2_85D	PCIEQ2	PCIE USB R2D C P
PCIE_USB_R2D	PCIEQ2_85D	PCIEQ2	PCIE USB R2D C N
PCIE_USB_D2R	PCIEQ2_85D	PCIEQ2	PCIE USB D2R P
PCIE_USB_D2R	PCIEQ2_85D	PCIEQ2	PCIE USB D2R N
PCIE_CLK100M_USB	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M USB P
PCIE_CLK100M_USB	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M USB N
PCIE_CLK100M_USB	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M USB C P
PCIE_CLK100M_USB	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M USB C N

## Ethernet MDI Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
RES	ENNET_MDI	ENNET_MDI_100D	ENNET_MDI	ENNETCONN MDI P<3..0>	26 27
RES	ENNET_MDI	ENNET_MDI_100D	ENNET_MDI	ENNETCONN MDI N<3..0>	26 27
RES	ENNET_MDI	ENNET_MDI_100D	ENNET_MDI	ENNETCONN MDI T P<3..0>	27
RES	ENNET_MDI	ENNET_MDI_100D	ENNET_MDI	ENNETCONN MDI T N<3..0>	27

## FireWire Net Properties

ELECTRICAL_CONSTRAINT_SECT		NET_TYPE		
		PHYSICAL	SPACING	
	FW_R0_TPA	FW_110d	FW_TP	FW PORT0 TPA P 29 30
	FW_R0_TPA	FW_110d	FW_TP	FW PORT0 TPA N 29 30
	FW_R0_TPB	FW_110d	FW_TP	FW PORT0 TPB P 29 30
	FW_R0_TPB	FW_110d	FW_TP	FW PORT0 TPB N 29 30

## USB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
	USB2_50m	USB2	USB HUB UP DP 31
	USB2_50m	USB2	USB HUB UP DM 31
	USB2_50m	USB2	USB DEV DP 31
	USB2_50m	USB2	USB DEV DM 31
	USB2_50m	USB2	USB DEV F DP 31
	USB2_50m	USB2	USB DEV F DM 31
	USB2_50m	USB2	USB HOST DP 31 32
	USB2_50m	USB2	USB HOST DM 31 32
	USB2_50m	USB2	USBIN1 H1 DP 31 33
	USB2_50m	USB2	USBIN1 H1 DM 31 33
	USB2_50m	USB2	USBIN2 H1 DP 31 33
	USB2_50m	USB2	USBIN2 H1 DM 31 33
	USB2_50m	USB2	USBIN3 H1 DP 31 33
	USB2_50m	USB2	USBIN3 H1 DM 31 33
	USB2_50m	USB2	USB UC DP 20 33
	USB2_50m	USB2	USB UC DM 20 33
	USB2_50m	USB2	USB AUDIO DP 11 33
	USB2_50m	USB2	USB AUDIO DM 11 33
	USB2_50m	USB2	USB CAMERA DP 10 33
	USB2_50m	USB2	USB CAMERA DM 10 33
	USB2_50m	USB2	CAM DP 10 48
	USB2_50m	USB2	CAM DM 10 48
	USB2_50m	USB2	AUD 161 USB DP 12
	USB2_50m	USB2	AUD 161 USB DM 12
	USB2_50m	USB2	DM1 33
	USB2_50m	USB2	DP1 33
	USB2_50m	USB2	DM2 33
	USB2_50m	USB2	DP2 33
	USB2_50m	USB2	DM3 33
	USB2_50m	USB2	DP3 33





